◉ Itautec

Brasília - DF, 07 de julho de 2006

CT/FGCO/172/2006

Ao
Tribunal Superior do Trabalho
Serviço de Licitações e Contratos
Brasília-DF

REF.: Pregão Eletrônico Nº 049/2006
Data de Abertura: 13/07/2006

Prezados (as) Senhores (as),

A Itautec S.A. - Grupo Itautec, no interesse em participar da licitação em referência vem solicitar esclarecimentos sobre os itens abaixo:

1. No Anexo I - Especificações Técnicas, está sendo solicitado para os microcomputadores dos itens 01 e 02:

   1.1. Memória Ram: "1GB - DDR2 400 MHz - SDRAM - suporte a dual channel 2 - MEMÓRIA RAM (implementado)".

   Perguntamos: A Tecnologia de memória DDR2 é exclusiva para microcomputadores com a plataforma Intel. Desta forma, visando proporcionar a participação de microcomputadores com plataforma AMD, solicitamos que também sejam aceitos equipamentos com tecnologia de memória do tipo DDR.

   1.2. Controladora de Vídeo: "128 MB de memória dedicada ou compartilhada dinamicamente (DVMT)".

   Perguntamos: A Tecnologia de compartilhamento dinâmico de memória (DVMT) é exclusiva para microcomputadores com a plataforma Intel. Desta forma, visando proporcionar a participação de microcomputadores com a plataforma AMD, solicitamos que também sejam aceitos equipamentos dotados de controladora de vídeo com tecnologia de compartilhamento de memória sem o recurso de compartilhamento dinâmico.

Abaixo informamos os dados da nossa empresa para possíveis contatos:
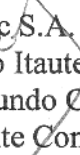
- Dados para contato - Filial Brasília - DF
- Contato: Jorge Ítalo Dimatteu Telles
- Endereço: SCS Q. 01 - Bloco "H" Ed. Morro Vermelho 3º Andar - CEP 70397-900
- Município/UF: Brasília-DF
- Telefone: (61) 3323-3031 Ramal: 1126 - (61) 9994-1076
- Fac-símile: (61) 3226-1251
- E-mail: italo@itautec.com.br

Itautec

Sem mais, colocamo-nos à disposição de V.Sas. para outras informações complementares que se façam necessárias.

Atenciosamente,

Itautec S.A.
Grupo Itautec
Maurício Martins de Oliveira Júnior
Analista de Sistemas

Itautec S.A.
Grupo Itautec
Raimundo Carlos Pereira
Gerente Comercial Regional

Assunto: Re: [Fwd: Pregão Eletrônico Nº 049/2006 - Solicitação de Esclarecimentos]
De: Henrique <jhrfilho@tst.gov.br>
Data: Mon, 10 Jul 2006 13:11:45 -0300
Para: Serviço de Licitações e Contratos <srlca@tst.gov.br>
CC: Mauricio Pena <mpena@tst.gov.br>, Lucio Mafra Martins Teixeira <mafra@tst.gov.br>, Luiz Antonio
Mendes Garcia <lgarcia@tst.gov.br>

Em anexo, as respostas aos questionamentos da Itautec.

Serviço de Licitações e Contratos escreveu:

> Sr. Diretor da SEPROD,
> Segue em anexo pedido de esclarecimento formulado ao Pregão Eletrônico 49/2006.
> Conforme regra estabelecida no Decreto nº 5.405/2005, art. 18, § 1º, resposta
> deverá ser formulada por este Pregoeiro em até 24 horas.
> Respeitosamente,

> **Assunto:**
>   Pregão Eletrônico Nº 049/2006 - Solicitação de Esclarecimentos
> **De:** Maurício Martins <mauricio.oliveira@itautec.com>
> **Data:** Fri, 7 Jul 2006 17:46:01 -0300
> **Para:** <cpl@tst.gov.br>
> **Para:** <cpl@tst.gov.br>
> **CC:** "'italo, Jorge Italo Dimatteu Telles'" <italo@itautec.com>

```
Prezado(as) Senhores(as),

Segue anexo os nossos questionamentos refente ao Edital citado acima.


Atenciosamente,

Maurício Martins de Oliveira Júnior
Itautec S.A
Regional Brasília
Tel.: (61) 3323-3031 - Ramal 1128
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```

Resposta Questionamento Itautec.doc	**Content-Type:** application/msword
	Content-Encoding: base64

Paper DDR2.pdf	**Content-Type:** application/pdf
	Content-Encoding: base64

1. No Anexo I - Especificações Técnicas, está sendo solicitado para os microcomputadores dos itens 01 e 02:

   1.1. Memória Ram: "1GB - DDR2 400 MHz - SDRAM - suporte a dual channel 2 - MEMÓRIA RAM (implementado)".

   Perguntamos: A Tecnologia de memória DDR2 é exclusiva para microcomputadores com a plataforma Intel. Desta forma, visando proporcionar a participação de microcomputadores com plataforma AMD, solicitamos que também sejam aceitos equipamentos com tecnologia de memória do tipo DDR.

RESPOSTA: Não conseguimos comprovar a validade da afirmação de que a tecnologia de memória DDR2 seja exclusiva para microcomputadores com a plataforma Intel. Anexamos um artigo descrevendo a tecnologia de memória DDR2, onde sequer é citado o nome Intel.
Inclusive, causa–nos estranheza, pois desde o ano passado os nossos editais para aquisição de microcomputadores, exigem a presença de memórias DDR2, e só agora isto está sendo questionado. Desta forma permanece a exigência de memórias DDR2.

   1.2. Controladora de Vídeo: "128 MB de memória dedicada ou compartilhada dinamicamente (DVMT)".

   Perguntamos: A Tecnologia de compartilhamento dinâmico de memória (DVMT) é exclusiva para microcomputadores com a plataforma Intel. Desta forma, visando proporcionar a participação de microcomputadores com a plataforma AMD, solicitamos que também sejam aceitos equipamentos dotados de controladora de vídeo com tecnologia de compartilhamento de memória sem o recurso de compartilhamento dinâmico.

RESPOSTA: No caso do equipamento não possuir o recurso de compartilhamento dinâmico, resta, conforme o texto do edital, a opção de "128 MB de memória dedicada", não inviabilizando a participação de outras plataformas.

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DDR2 Offers New Features and Functionality

DDR2 SDRAM introduces features and functions that go beyond the

DDR SDRAM specification and enable DDR2 to operate at data rates of 400 MHz,

533 MHz, 667 MHz, and above. The advancements of DDR2 are largely the result

of changes in DRAM architecture and signaling, as well as additions to the mode

register for lower power and improved command/data bandwidth. This article discusses the various changes and the resulting features and benefits of DDR2 technology.

DDR2

- *400 MHz and beyond*
- *Higher bandwidth*
- *Lower power*

DRAM Architecture Changes

DDR2 Array Definition

Changes to the DRAM architecture include shortened page size for reduced activation power, burst lengths of four and eight for improved data bandwidth capability, and the addition of eight banks in 1Gb densities and above.

DDR2 Page Size

Page size is important to the power consumption of a DRAM device. Page size is defined as the minimum number of column locations that are accessed with a single ACTIVATE command. This is calculated as the number of column locations times the number of DQs on the DRAM. For example, the 512Mb, x8 DDR2 SDRAM has 1,024 column locations, so the page size is 1,024 columns times 8 DQs, which equals 8,192 bits. Dividing the 8,192 bits by a word length of 8 equals 1,024 bytes or 1KB.

Each time an ACTIVATE command is given, all bits in the page are read by the sense amplifiers and restored to the correct value. Because this process is a major contributor to the active power, a device with a shorter page size has a significantly lower operating current. The page size of the 512Mb DDR2 device is half that of a standard DDR SDRAM. Therefore, the current consumed by the ACTIVATE commands is greatly reduced, resulting in improved $I_{DD}0$, $I_{DD}1$, and $I_{DD}7$ specifications. (See Table 1 for a comparison of DDR2 and DDR page size and number of banks.)

With the higher-density DDR2 SDRAM (512Mb, 1Gb, and 2Gb), the page size increases on the x16 device. The x4 and x8 devices continue to operate at lower activate currents with a 1KB page size, similar to the 256Mb DDR2 SDRAM. However, the x16 DDR2 page size increases to 2KB. While power consumption

Table 1: DRAM Architectures

Density		DDR	DDR2
256Mb	Page Size	1KB	1KB
	Banks	4	4
512Mb	Page Size	2KB	1KB (x4, x8), 2KB (x16)
	Banks	4	4
1Gb	Page Size	2KB	1KB (x4, x8), 2KB (x16)
	Banks	4	8
2Gb	Page Size	–	1KB (x4, x8), 2KB (x16)
	Banks	–	8

increases on the x16 DDR2 SDRAM, system power is typically no higher than that of the x8 device. A 64-bit bus requires eight x8 DRAM devices to support the bus width, while only four x16 DRAM devices are required. Thus, the activate current of a x16 component may be somewhat higher, but the overall system power consumption is still lower.

DDR2 Bank Accesses

Another change from DDR to DDR2 (as shown in Table 1) is the number of banks on the larger-density DDR2 devices. A typical four-bank access, which is applicable to the 256Mb and 512Mb DDR2 SDRAM, is shown in Figure 1. Bank accesses for DDR2 devices are similar to DDR, except ACTIVATE command spacing is 7.5ns for 1KB and 10ns for 2KB page size, due to the increased power consumption of the larger page size. When a bank is precharged, it may be activated again after ^tRC is met, following the original ACTIVATE command.

The larger-density 1Gb and 2Gb DDR2 devices use eight banks, which increases flexibility in DRAM accesses. However, it also increases the power that must be delivered to the DRAM. To keep the power
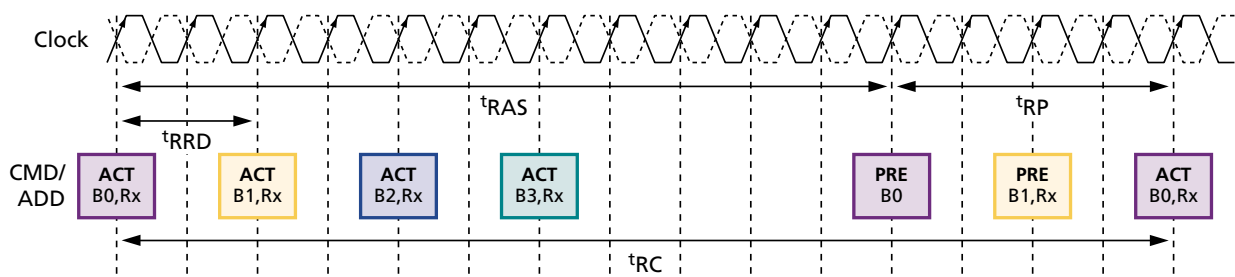
Figure 1: ACTIVATE for Four-Bank DDR or DDR2 Devices

Note: tRRD is 7.5ns on 1KB page size and 10ns on 2KB page size (two clock minimum).
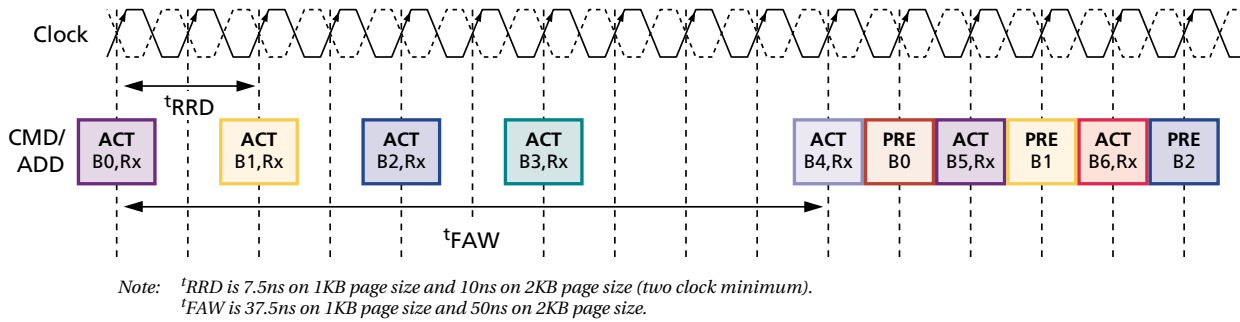tFAW is 37.5ns on 1KB page size and 50ns on 2KB page size.

Figure 2: ACTIVATE for Eight-Bank DDR or DDR2 Devices

delivery from adversely affecting the functionality of the DRAM and the memory subsystem, an additional restriction (^{t}FAW) is applied to bank ACTIVATE commands, as shown in Figure 2. ACTIVATE-to-ACTIVATE spacing remains ^{t}RRD, as in the four-bank case; however, there is an additional restriction within any ^{t}FAW window where no more than four banks may be activated. This requires a short amount of extra time prior to activating the fifth bank.

Signaling Features

On-Die Termination

On-die termination (ODT) has been added to the DDR2 data signals to improve signal integrity in the system. Figure 3 shows a functional diagram of the on-die termination. The termination value of R$_{TT}$ is the Thevinen equivalent of the resistors that termi-nate the DQ inputs to VssQ and V$_{DD}$Q. An ODT pin is added to the DRAM so the system can turn the termination on and off as needed. In a simple system with one DRAM load per DQ signal, the termination is turned on for WRITEs and disabled for READs.

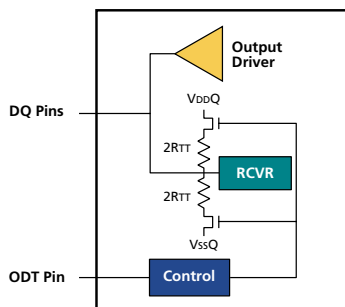Figure 4 shows the ODT trace routing on a typical PC system with two memory slots. Each slot contains two ranks of memory (front and back). A separate ODT signal is routed to each rank of memory to provide flexibility in power management and the best system performance. The routing of ODT signals is similar to the routing of CS# signals.
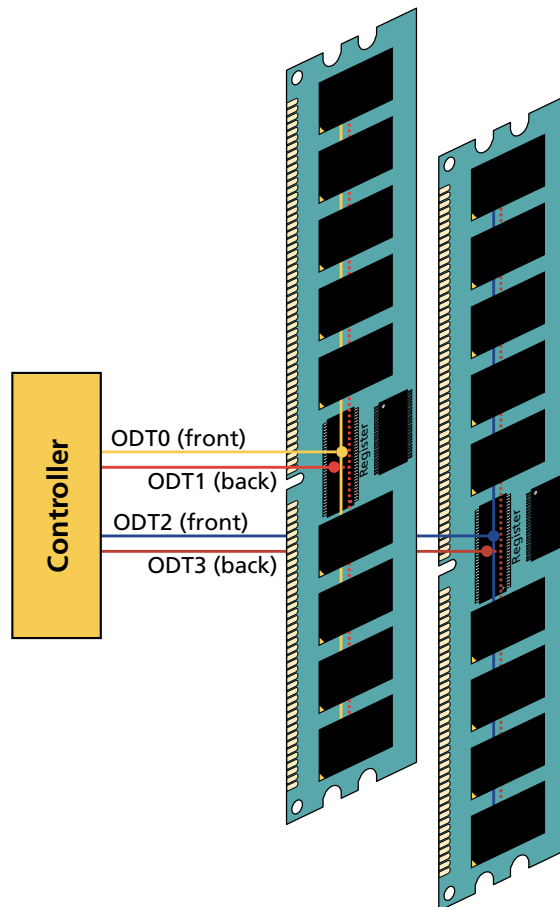

Figure 3: Functional Diagram for On-Die Termination

Figure 4: Typical 2-Slot ODT Routing

ODT WRITEs

Figure 5 shows a typical termination scheme for write data in a two-module system. If only one module is loaded in the system, a 150 ohm equivalent termination (300 ohm pull-up/300 ohm pull-down) must be enabled on the module during the WRITE. If two modules are loaded into the system, the termination on the module not receiving the write data should be enabled at 75 ohm equivalent termination resistance (150 ohm pull-up/150 ohm pull-down). This termination scheme provides optimal trade-offs between signal integrity and voltage swing.

The equivalent comparison for write data at 533 MT/s is shown in Figure 6. Neither bus has significant overshoot. However, the voltage margin on the SSTL bus is not sufficiently outside the DRAM input voltage requirements. Thus, when the input slew rate starts slowing down in the two-slot system, the data eye that the DRAM must capture is significantly reduced. The ODT system shows increased voltage margin, and the data eye remains significantly larger, even under more heavily loaded conditions.
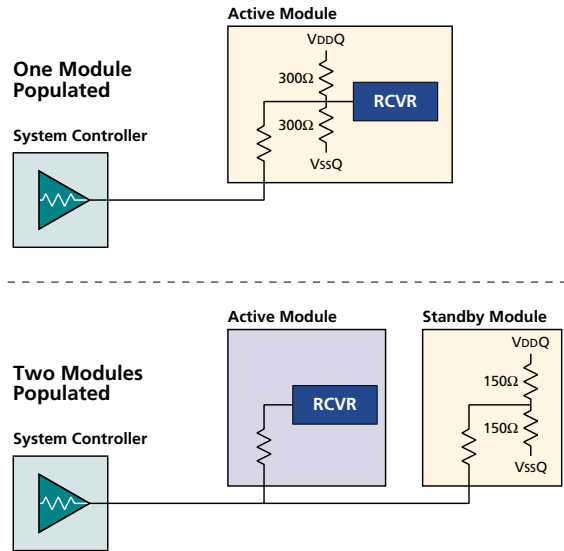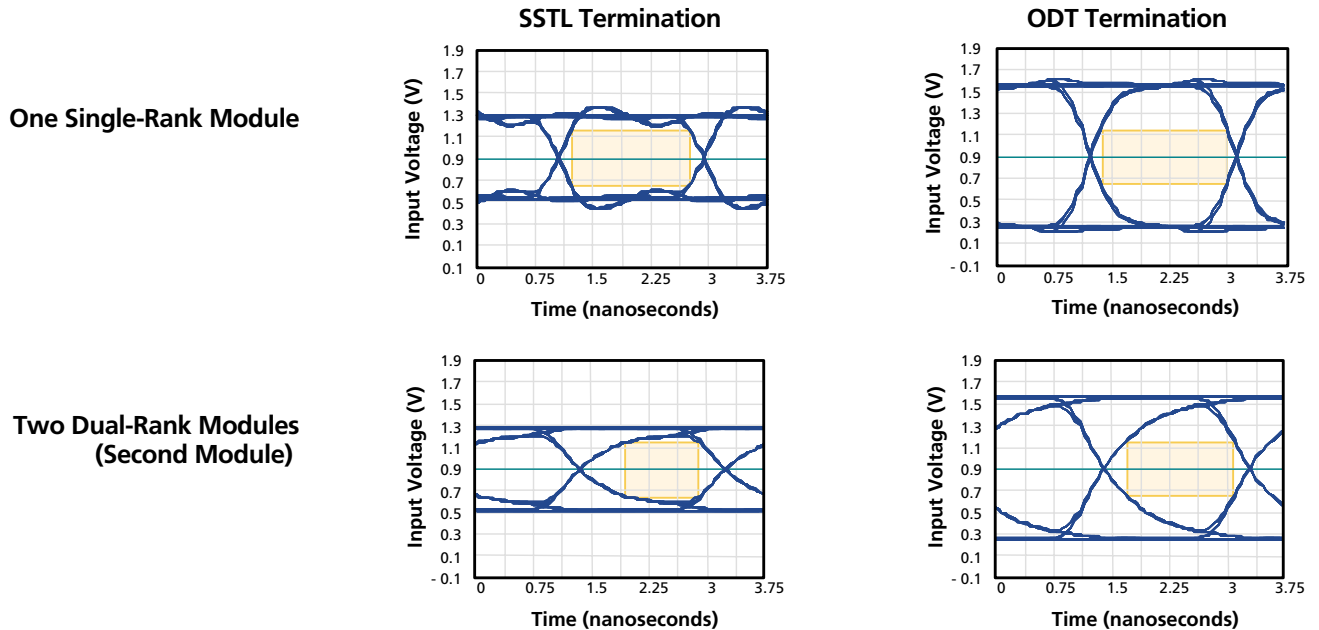

Figure 5: Typical ODT Configuration for DRAM WRITEs

Figure 6: ODT vs. SSTL Termination Comparison for WRITEs

ODT READs

Figure 7 shows a typical termination scheme for read data in a two-module system. For READs, on-die termination must be included on the controller. If only one module is loaded in the system, a 75 ohm termination should be enabled on the system controller. If two modules are loaded, the controller termination should be increased to 150 ohms and the unused module should terminate at 75 ohms. This configuration provides good voltage margin at the controller.

Figure 8 shows a comparison of a DDR2 DQ bus for a typical SSTL-terminated, two-module system using ODT termination versus a non-ODT system reading data at 533 MT/s. The most obvious difference between the two buses is the reduction in the overshoot on the data bus. The overshoot reduction significantly improves the voltage margin and reduces inter-symbol interference (ISI). The second major improvement using DDR2 ODT is the increase in the slew rate in the two-module case. The SSTL bus starts "laying over" when more loads are added, which detracts from the timing margin in the system. Both of these improvements dramatically increase the size of the data eye that the system controller must capture to read data from the DRAM.
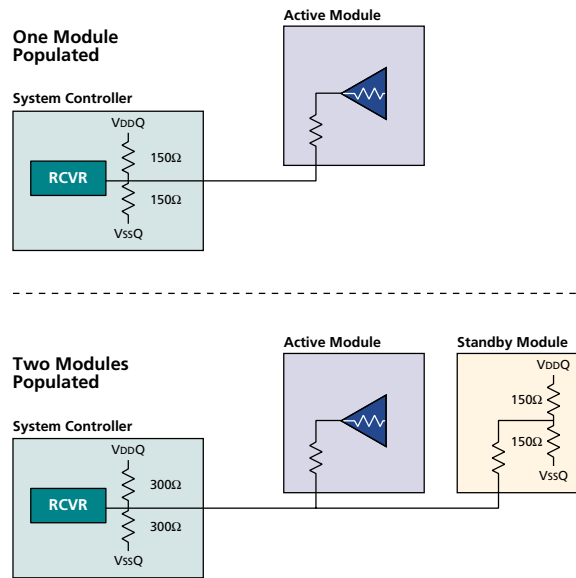

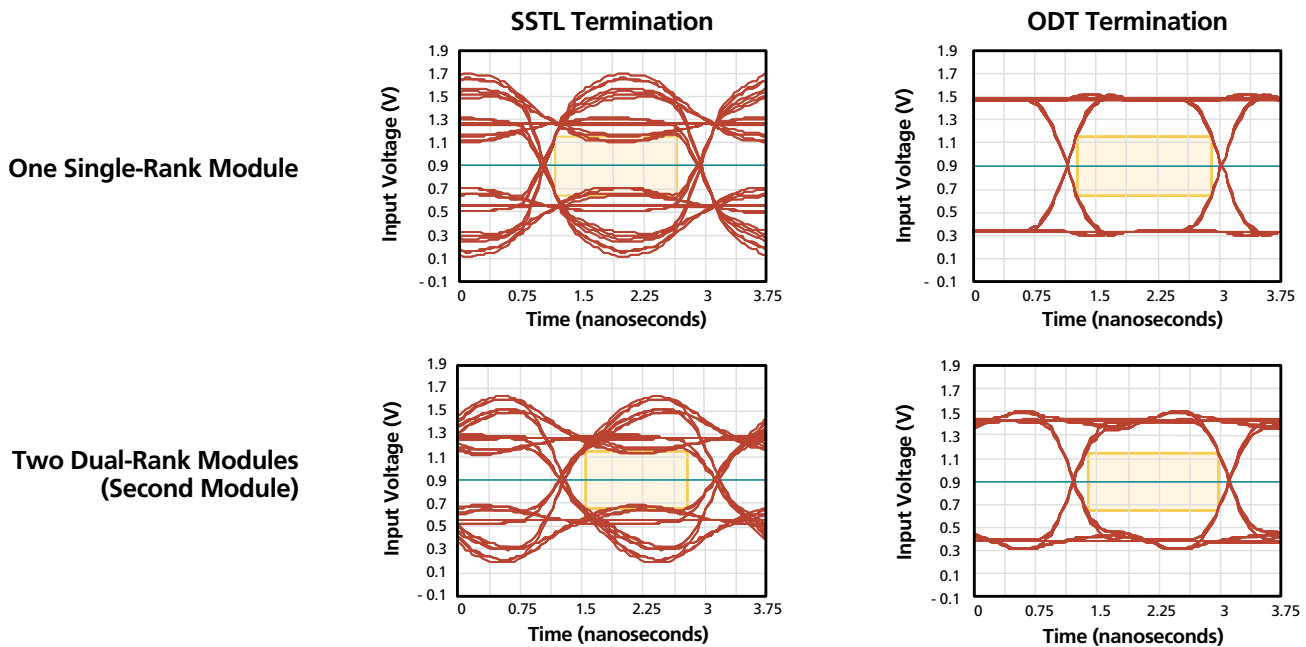**Figure 7: Typical ODT Configuration for DRAM READs**

Figure 8: ODT vs. SSTL Termination Comparison for READs

Overall, ODT implementation provides improved signal integrity, data eyes, and voltage margin for DDR2 to enable systems to attain higher data rates. At the same time, it is an option and can be disabled for systems that require a more traditional SSTL-type of bus.

Termination Values

As illustrated in Figures 5 and 7, on-die termination can have different values, depending on the system configuration. This is controlled via the extended mode register (EMR). (See Figure 9.) If extended mode bits 2 and 6 are both "0," the on-die termination is disabled on the DRAM. Two additional options include selecting either an RTT equivalent value of 75 ohms (150 ohms pull-up and 150 ohms pull-down) or an RTT equivalent of 150 ohms (300 ohms pull-up and 300 ohms pull-down). The proper termination value is selected to optimize signal integrity at minimum power, as shown in Figures 6 and 8.

On-Die Termination Control in Active Mode

After the proper value of termination is selected, the system controller must switch the termination on and off at the proper times. While the DRAM is in active or fast exit power-down mode, the termination turns on two clock cycles after the ODT signal is registered HIGH, as shown in Figure 10. For module 2, the ODT signal is latched HIGH on the same clock cycle as the READ command to module 1. Two clock cycles later, the on-die termination on the module 2 DRAM turns on. To schedule on-die termination, ODT should be transitioned HIGH three clocks before the data is on the bus to ensure it is on prior to the preamble.

To disable on-die termination, the ODT signal must be registered LOW by the clock. Then, two and a half cycles later, the termination turns off, as shown in Figure 10. The extra half cycle allows the termination to remain enabled until after the data has stopped driving on the bus. Thus, the ODT pin can be registered LOW two clock cycles prior to the end of the data burst on the bus.

On-Die Termination Control in Power-Down

Asynchronous operations are also associated with the ODT pin when the DRAM is in slow exit active power-down or precharge power-down mode. During this operation, the turn on and off time is an analog delay off the registration of the ODT signal. The timing isn't as critical since data can't be read from or written to a rank that is in power-down mode.

BA1 BA0 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0 **Address Bus**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EMR		0*	out	RDQS	DQS#	OCD Program			RTT	Posted CAS			RTT	ODS	DLL

*E13 (A13) is reserved for future use and must be programmed to "0".

Extended Mode Register

E6	E2	RTT (nominal)
0	0	RTT disabled
0	1	75 ohms
1	0	150 ohms
1	1	Reserved

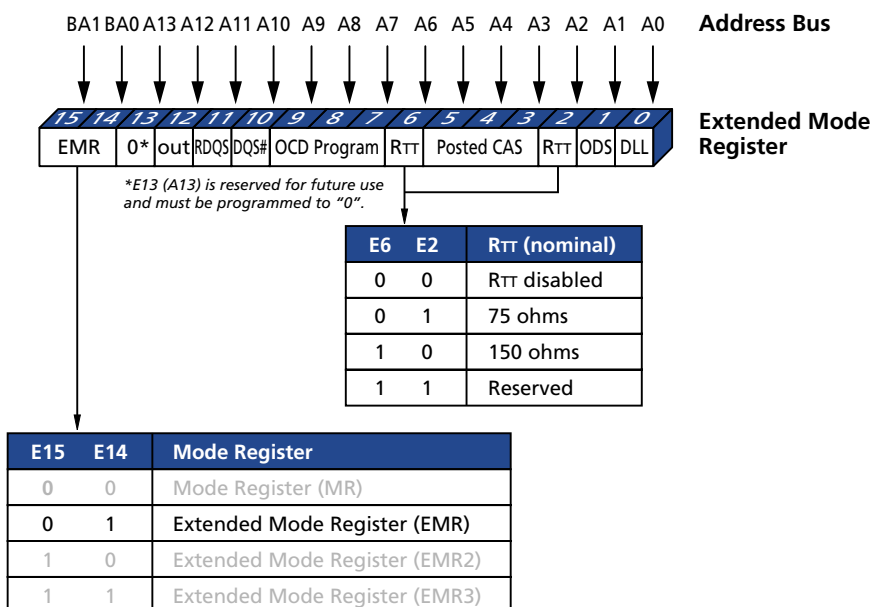| E15	E14	Mode Register
0	0	Mode Register (MR)
0	1	Extended Mode Register (EMR)
1	0	Extended Mode Register (EMR2)
1	1	Extended Mode Register (EMR3)

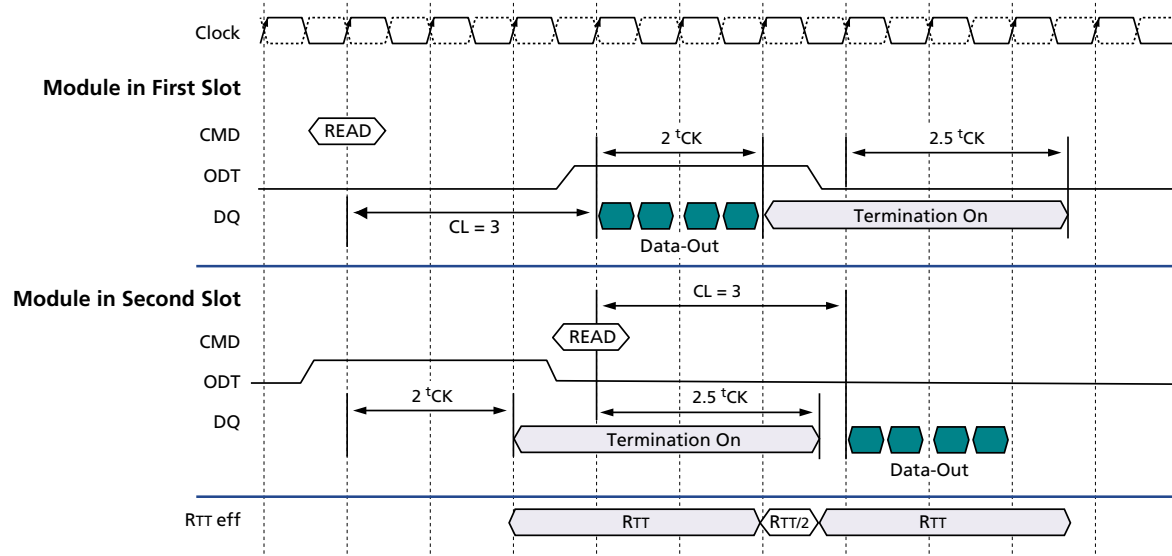**Figure 9: Extended Mode Register Control for On-Die Termination**

Figure 10: Rank-to-Rank ODT Control – READs

Thus, the system only has to enable the termination to form a window around the data from the other ranks. See the DDR2 data sheet for additional information on specific ODT timings and restrictions.

On-Die Termination Control in Self Refresh

During self refresh, the DRAM disables on-die termination and ignores the ODT pin, regardless of the values programmed into the EMR. A memory subsystem that is in self refresh mode cannot read or write data, so disabling on-die termination does not affect signal quality, and it allows the DRAM to minimize power consumption.

Off-Chip Driver (OCD) Calibration

DDR2 also contains an off-chip driver (OCD) calibration to reduce the mismatch between pull-up and pull-down output driver characteristics, which can improve the system timing margin. Without OCD calibration, the DRAM has a nominal output driver strength of 18 ohms ±30% and a pull-up and pull-down mismatch of up to 4 ohms. Using OCD calibration, a system can reduce the pull-up and pull-down mismatch and target the output driver at 18 ohms to optimize the signal integrity. OCD calibration is performed by the LOAD MODE command using the EMR, which enables the DRAM to be in OCD drive mode with the outputs driving HIGH or LOW, or the DRAM can be in OCD adjust mode. A system that is not using OCD calibration can enable a default output drive strength of 18 ohms ±30% by selecting the OCD default setting (see Figure 11).

For a system to utilize OCD calibration, a LOAD MODE command must be issued to the DRAM to enter drive mode by driving a HIGH or a LOW, as shown in Figure 12. When OCD drive mode is entered, the outputs drive the desired HIGH or LOW against the system termination until an OCD exit mode command is issued.

While the DRAM is in OCD drive mode, the system controller must measure the voltage it receives against a known reference. If the voltage and termination values of a system are known, the DRAM output drive strength for pull-up and pull-down can be calculated separately. If the pull-up and/or pull-down drive strength is not at 18 ohms, the system controller can enter OCD adjust mode and increase or decrease the drive strength of the DRAM, using the sequence shown in Figure 13.
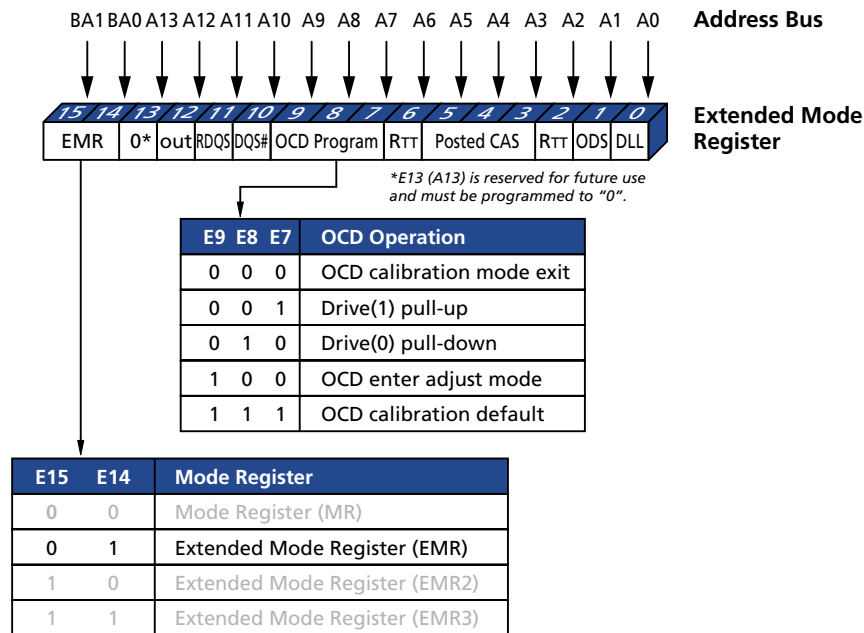
Figure 11: Extended Mode Register Control for OCD Calibration

E9	E8	E7	OCD Operation
0	0	0	OCD calibration mode exit
0	0	1	Drive(1) pull-up
0	1	0	Drive(0) pull-down
1	0	0	OCD enter adjust mode
1	1	1	OCD calibration default

E15	E14	Mode Register
0	0	Mode Register (MR)
0	1	Extended Mode Register (EMR)
1	0	Extended Mode Register (EMR2)
1	1	Extended Mode Register (EMR3)

E13 (A13) is reserved for future use and must be programmed to "0".

During OCD adjust mode, the memory controller issues a WRITE with a burst length of four to DQ0–DQ3 to adjust the pull-up or pull-down. To maintain commonality across different DRAM widths (x4, x8, x16), the adjust data is always entered on DQ0–DQ3. Refer to the DDR2 data sheet for details on the available adjust mode op-codes.

Using OCD calibration, it is possible for the DRAM to set the output drive strength at 18 ohms ±1.5 ohms. However, in actual systems, the system error of the reference voltages, termination, and comparators must be added to this variation, which will decrease the output drive accuracy in most systems. The OCD calibration is only intended to help
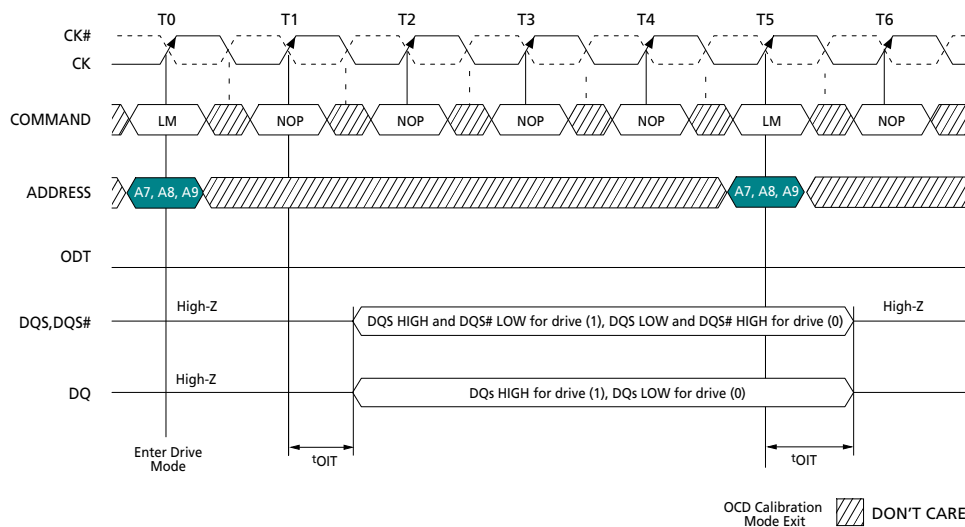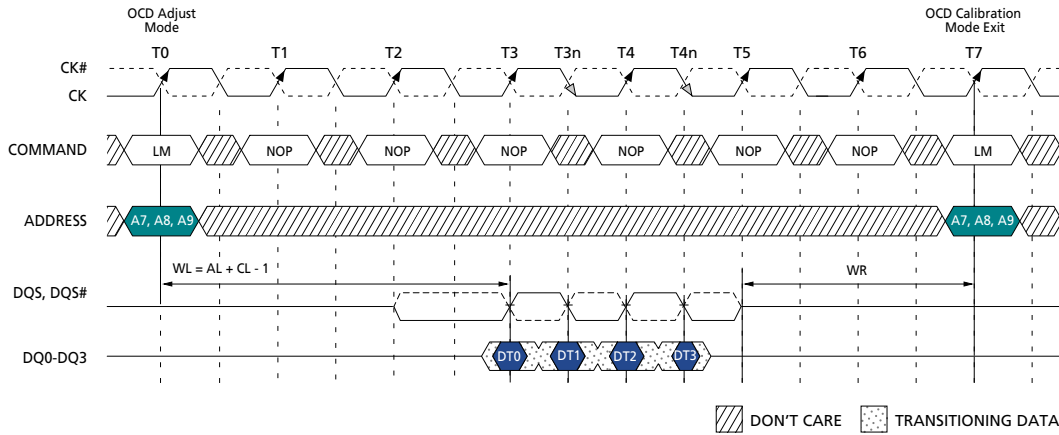

Figure 12: OCD Driver Mode

Figure 13: OCD Adjust Mode

match the output driver pull-up and pull-down to 18 ohms at nominal temperature and voltage conditions. Using this feature to move the drive strength higher or lower than 18 ohms is not supported. OCD is only supported for the full-strength output driver option and is not supported in half-strength mode. More specific details regarding OCD adjust mode can be found in the DDR2 data sheet.

Additional Mode Register Changes

Mode Register (MR)

Some of the additional features and functionality that have been added to DDR2 require changes in the mode register and the extended mode register.

Figure 14 highlights the changes made in the mode register for DDR2. These include support for burst lengths of 4 and 8 only, a modification of the sequential interleave mode, and extension of the CAS
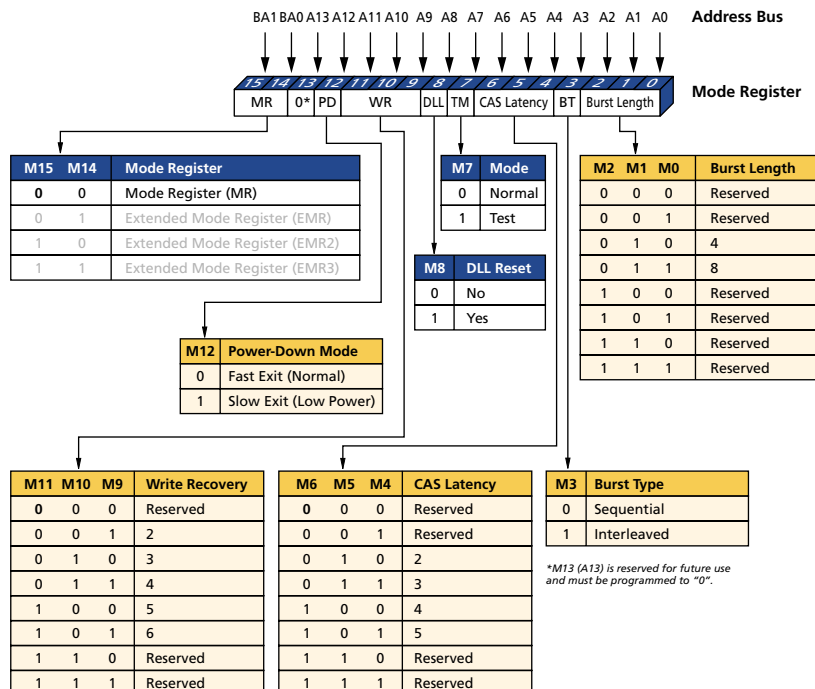

M15	M14	Mode Register
0	0	Mode Register (MR)
0	1	Extended Mode Register (EMR)
1	0	Extended Mode Register (EMR2)
1	1	Extended Mode Register (EMR3)

M7	Mode
0	Normal
1	Test

M2	M1	M0	Burst Length
0	0	0	Reserved
0	0	1	Reserved
0	1	0	4
0	1	1	8
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

M8	DLL Reset
0	No
1	Yes

M12	Power-Down Mode
0	Fast Exit (Normal)
1	Slow Exit (Low Power)

M11	M10	M9	Write Recovery
0	0	0	Reserved
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	Reserved
1	1	1	Reserved

M6	M5	M4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	Reserved
1	1	1	Reserved

M3	Burst Type
0	Sequential
1	Interleaved

*M13 (A13) is reserved for future use and must be programmed to "0".

Figure 14: Mode Register Changes for DDR2

latencies supported. In addition, a low-power defini-tion for active power-down mode and a write recovery parameter have been added.

CAS Latency

DDR2 operates at higher clock frequencies than DDR SDRAM. Figure 15 illustrates the difference between a DDR READ at a 266 MHz data rate and a DDR2 READ at a 533 MHz data rate. The latency of each device is the same, approximately 15ns. For the DDR SDRAM, this is equivalent to two clocks; for DDR2, four clocks.

As clock rates increase, the number of latencies supported must also increase. Table 2 shows the latencies supported for various clock rates and CAS latencies. The DRAM latency is calculated as ^tCK * *CAS latency supported*. DDR2 is targeted at latencies of 12ns–20ns. If the DRAM latency is beyond this range, it is unlikely that a system will utilize that latency due to lost system performance. Likewise, it is unlikely the DRAM will meet latencies below 12ns due to DRAM core performance. To support DDR2's higher clock rates, the CAS latency programmability has been set at three to five clocks. Half clock latencies are not supported.

WRITE Latency

DDR2 also includes a modification to the WRITE latency specification. Figure 16 illustrates the differ-ences between DDR and DDR2 SDRAM. DDR SDRAM

Table 2: DDR2 READ Latencies

$^{RL}_{\,^tCK}$	READ Latency (clocks)		
	3	**4**	**5**
DDR2-400 5ns	15ns	20ns	25ns
DDR2-533 3.75ns	11.25ns	15ns	18.75ns
DDR2-667 3ns	9ns	12ns	15ns
DDR2-800 2.5ns	7.5ns	10ns	12.5ns

☐ Unlikely operation

has a WRITE latency of one clock, which means that approximately one clock after a WRITE command, the DRAM starts clocking in data. However, given the increase in clock rates, this time is very short, making it difficult for the DRAM to prepare to capture data. DDR2 enables the WRITE latency to track the CAS latency minus one clock.

Figure 16 shows a 533 MHz DDR2 device with CAS latency set to four clocks. The WRITE latency is set to *CAS latency – 1 clock,* which is three clocks.

The modification in WRITE latency allows more time for DRAM input buffers to support higher clock frequencies. Additionally, tracking WRITE latency with CAS latency simplifies system read-to-write timings.
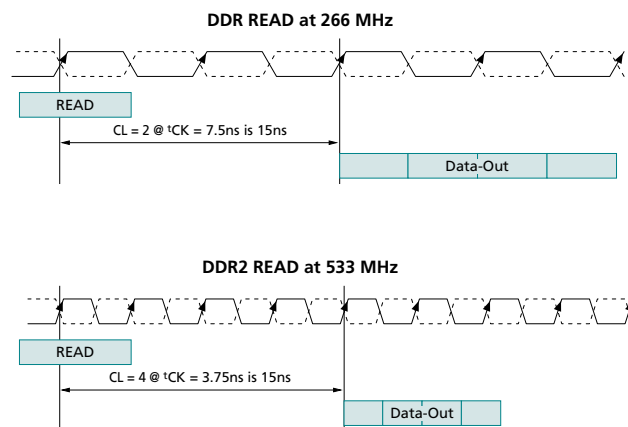
DDR READ at 266 MHz

READ

CL = 2 @ ^tCK = 7.5ns is 15ns

Data-Out

DDR2 READ at 533 MHz

READ

CL = 4 @ ^tCK = 3.75ns is 15ns

Data-Out

Figure 15: DDR2 vs. DDR READ

DDR WRITE at 266 MHz

WRITE

Equivalent WL = 1 @ ^tCK = 7.5ns is 7.5ns

Data-In

DDR2 WRITE at 533 MHz

WRITE

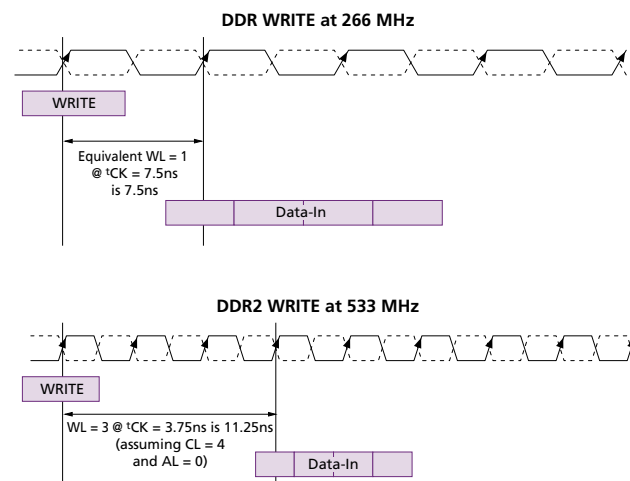WL = 3 @ ^tCK = 3.75ns is 11.25ns (assuming CL = 4 and AL = 0)

Data-In

Figure 16: DDR2 vs. DDR WRITE

Table 3: Sequential Burst Ordering

Burst Length	Starting Column (A2, A1, A0)	Order of Accesses Within a Burst Burst Type = Sequential	
		DDR	DDR2
4	0 0 0	0,1,2,3	0,1,2,3
	0 0 1	1,2,3,0	1,2,3,0
	0 1 0	2,3,0,1	2,3,0,1
	0 1 1	3,0,1,2	3,0,1,2
8	0 0 0	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7
	0 0 1	1,2,3,4,5,6,7,0	1,2,3,0,5,6,7,4
	0 1 0	2,3,4,5,6,7,0,1	2,3,0,1,6,7,4,5
	0 1 1	3,4,5,6,7,0,1,2	3,0,1,2,7,4,5,6
	1 0 0	4,5,6,7,0,1,2,3	4,5,6,7,0,1,2,3
	1 0 1	5,6,7,0,1,2,3,4	5,6,7,4,1,2,3,0
	1 1 0	6,7,0,1,2,3,4,5	6,7,4,5,2,3,0,1
	1 1 1	7,0,1,2,3,4,5,6	7,4,5,6,3,0,1,2

☐ Different

Sequential Interleave

To support the high data rates of DDR2, the DRAM must have the flexibility to prefetch four bits of data from the core instead of only two. Consequently, support for a burst length of two has been dropped. Prefetching four bits, however, makes it difficult to support the traditional sequential interleave mode for DRAM burst lengths of eight.

The sequential burst orders for DDR2 are shown in Table 3. For burst lengths of four, there is no change from the DDR specification. However, for burst lengths of eight, a new burst type called sequential nibble is implemented. During sequential nibble operation, the DRAM breaks the eight-bit burst into two separate four-bit nibbles. The sequential interleave is executed on the nibble with the starting column location, followed by a similar sequential interleave on the other nibble using the starting location that is equal to the lower bits of the starting column.

Using the nibble sequential burst, a system requiring sequential interleave can take advantage of the eight-bit burst and still use any starting column within the burst.

The interleave burst ordering for DDR2 is the same as DDR.

Active Power-Down Mode

Active power-down mode enables a system designer to optimize power and performance. In this mode, the transition timing between power-down exit and the next command is dependent upon the power-down mode bit.

If the power-down mode is set to fast exit mode, there is a two-clock delay from active power-down exit to any command (including READ). Alternatively, the power-down mode bit may be set to slow exit mode, which extends the power-down exit delay to six clocks, minus the additive latency to a READ command. Active power-down slow exit is the same as the precharge power-down time during all operations of the DRAM. The power-down mode bit is ignored in precharge power-down.

Write Recovery

Write recovery (WR) must be correctly entered into the mode register to ensure proper DRAM

Table 4: DDR2 Low-Power Mode Options

	MR (bit 12)	PD Mode	Delay from CKE HIGH to Command
Active Power-Down	0	Fast Exit	2 clocks to READ command
	1	Slow Exit	2 clocks to any non-READ command (Additive latency – 6 clocks) to READ
Precharge Power-Down	Ignored		2 clocks to any non-READ command (Additive latency – 6 clocks) to READ

NOTE: 1. Burst length = 4, additive latency = 0, and WRITE latency = 2.
2. Enable auto precharge.
3. WR is programmed via EMR [11,10,9] and is calculated by dividing ^tWR (ns) by ^tCK and rounding up to the next integer value.
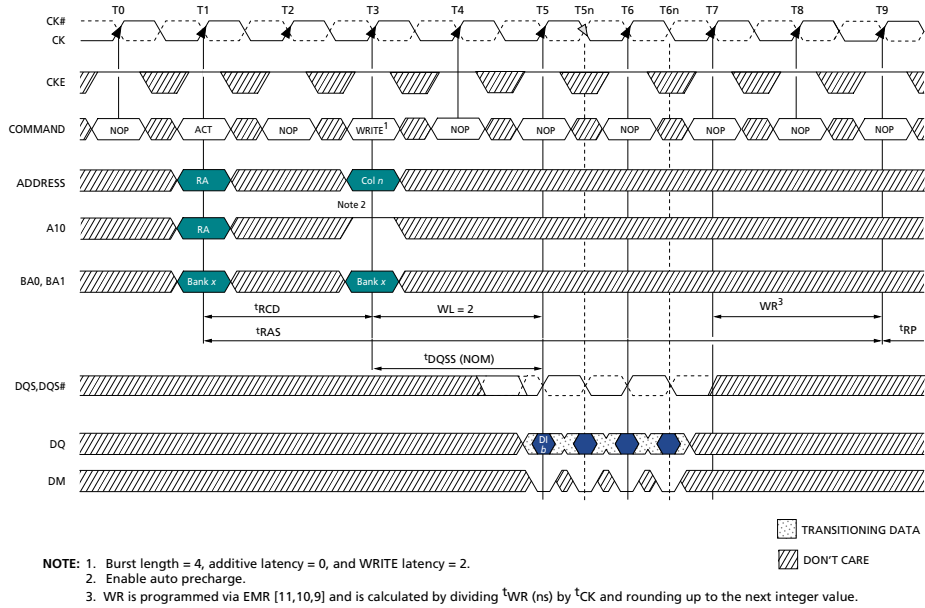
Figure 17: DDR2 Write-to-Precharge Timing

operation. Write recovery is measured from the end of write data to the time when the internal auto precharge operation starts (see Figure 17). To correctly set the MR, WR is calculated as $^tWR/^tCK$, rounded up to the next integer.

Extended Mode Register (EMR)

Additional enhancements have been made to the EMR, as shown in Figure 18. ODT and OCD calibration have been discussed previously. Other enhancements include additive latency, output disable, and DQ strobe configurability.
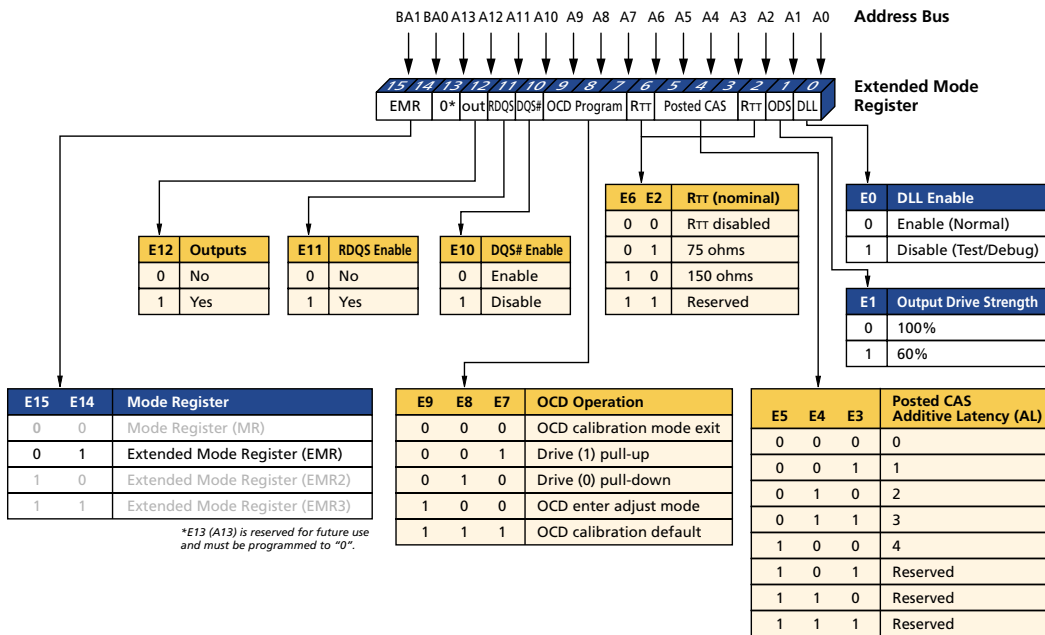
Figure 18: Extended Mode Register

Additive Latency

Figure 19 shows an example of DDR2 bank interleave READs. During these accesses, a bank is opened with an ACTIVATE command. After ^{t}RCD is met, a READ with auto precharge command is issued and data is read out of the DRAM. As seen in Figure 19, there are times when a command cannot be issued at the optimal location because there is another command already there. For example, ACT (to bank 2) must be delayed by one clock because the RD_AP (to bank 0) is already in that spot. The result is a gap in the output data.

To improve system scheduling, DDR2 includes a mode register for additive latency. Using additive latency, the DRAM captures READ or WRITE commands but waits to execute them until the additive latency time expires.

Figure 20 illustrates DRAM operation with two different additive latencies. The top figure shows an operation similar to DDR SDRAM using *AL = 0 clocks*. The bottom figure shows *AL = ^{t}RCD - 1 clock*. In this configuration, the ACTIVATE and READ commands can be issued back-to-back. The DRAM holds the
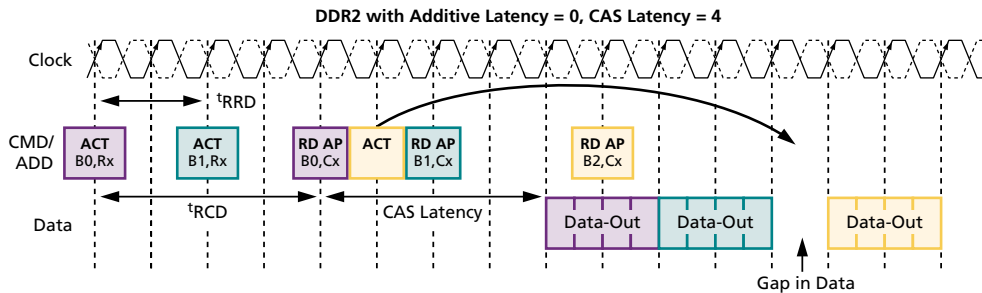
DDR2 with Additive Latency = 0, CAS Latency = 4

Figure 19: DDR2 READs With no Additive Latency

DDR2 with Additive Latency = 0

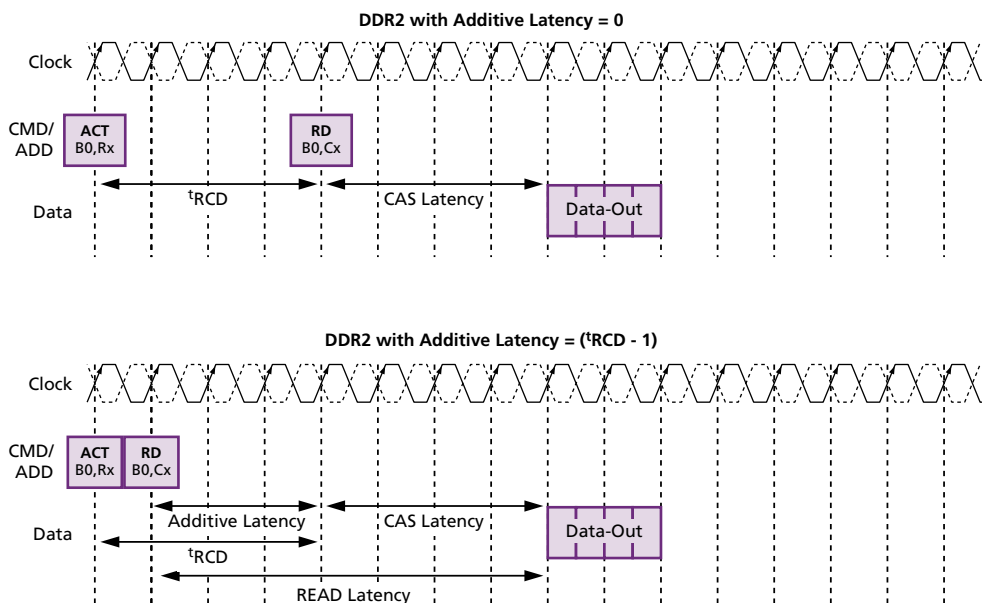**DDR2 with Additive Latency = (^{t}RCD - 1)**

Figure 20: DDR2 With Additive Latency

READ command for the additive latency time and then executes it on the same clock as the top diagram.

With additive latency set to $^tRCD - 1\ clock$, a simplified read system timing can be attained. Figure 21 assumes $^tRCD = 4\ clocks$. Thus, additive latency is set to three clocks. This allows the READ command to directly follow the ACTIVATE command. With a burst length of four, which requires two clocks to burst data, the two clocks for the back-to-back ACT and RD_AP commands match perfectly, enabling data to be continuously output from the DRAM without gaps. The simplicity of system bus scheduling is expected to be particularly popular in applications that have high page misses.

DQS Configuration

The extended mode register also allows configuration of the DQ strobes for multiple system configurations. Figure 22 highlights the areas of the extended mode register that configure the strobes. Bit 10 switches the strobes between differential and single-ended mode, and bit 11 can be used to enable the redundant strobe on the x8 device.

Single/Differential Data Strobe

DDR2 supports single-ended strobes in the same manner as DDR SDRAM, as shown in Figure 23.

DDR2 SDRAM also supports differential strobes. If differential strobes are enabled, DQS operates the same as in single-ended mode with the addition of
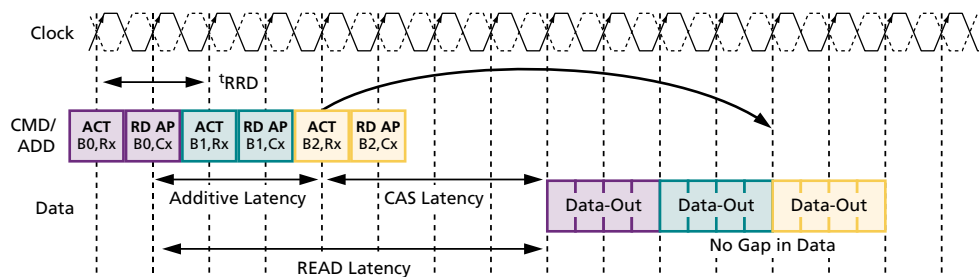

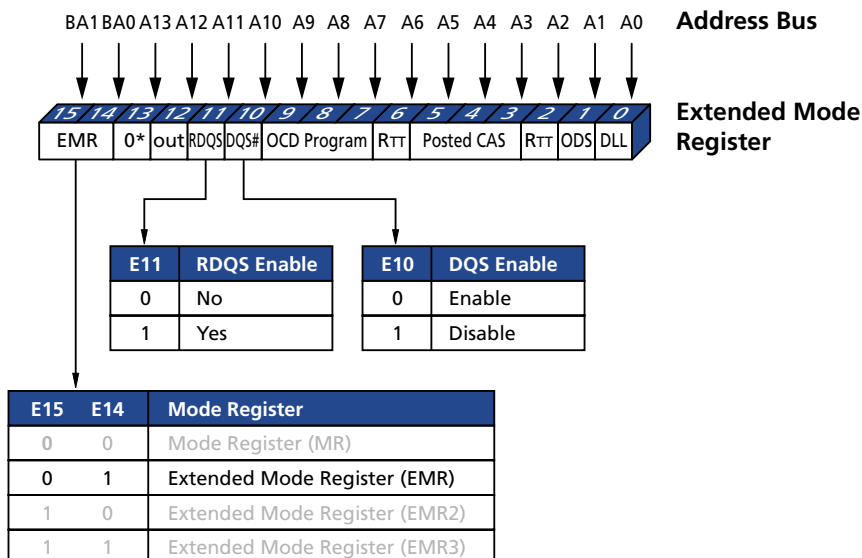**Figure 21: DDR2 READs Using Additive Latency**

E11	RDQS Enable
0	No
1	Yes

E10	DQS Enable
0	Enable
1	Disable

E15	E14	Mode Register
0	0	Mode Register (MR)
0	1	Extended Mode Register (EMR)
1	0	Extended Mode Register (EMR2)
1	1	Extended Mode Register (EMR3)

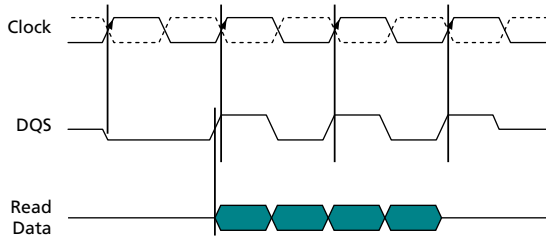**Figure 22: Extended Mode Register for DQS Configuration**

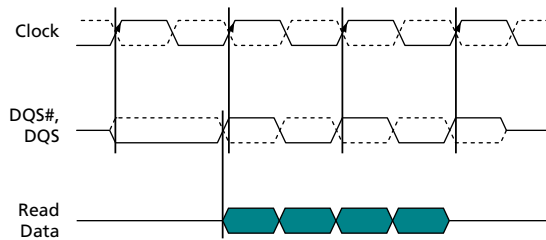**Figure 23: Single-Ended Strobe**

Figure 24: Differential Strobe

DQS# operating as the complement in differential signals. For READs the DRAM will output both signals, as shown in Figure 24. For WRITEs, the system must provide both input signals.

The use of differential strobes is system-dependent and may enable improved system timings due to reduced crosstalk and less simultaneous switching noise on the strobe output drivers.

Redundant DQS (RDQS)

The RDQS option is only available on the x8 DRAM and is required when mixing x4 and x8 DRAM devices in the same system. An example of this is shown in Figure 25. Because the x8 DRAM has only one DQS input for the 8-bit byte and the x4 has a DQS for each 4-bit nibble, the loading of the DQS lines is different when the devices are mixed in the same system.

RDQS reduces this effect. If devices are mixed in the system, the signal routing from the second x4 DRAM is routed to the RDQS pin on the x8 DRAM.
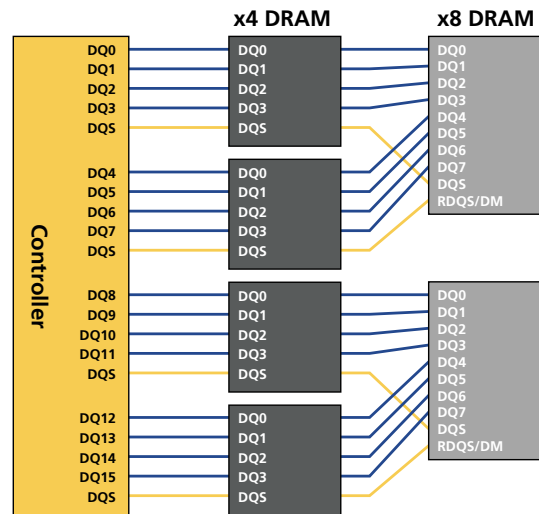

Figure 25: x4 and x8 Devices in Same System

During WRITEs, the loading and termination on the RDQS is the same as the DQS signals, so all signaling is matched for the x4 DRAMs. For READs, the x8 DRAM drives the RDQS output the same way it does the DQS. Thus, the controller can use RDQS to capture read data on a nibble device and the x8 DRAM emulates the functionality of the x4.

Systems mixing x4 and x8 devices can utilize RDQS signals to improve timing. RDQS functionality is only an option on the x8 DRAM. Additionally, if RDQS is enabled, the data mask functionality of the x8 DRAM is disabled.

Output Disable

For DDR SDRAM, it can be difficult to measure I_{DD} values in system environments. All I_{DD} values are specified with $I_{OUT} = 0mA$, which is challenging to accomplish in the system. Thus, DDR2 has an option to disable the output drivers from the EMR. If the output disable option is set, the last stage of the output driver is disabled. WRITEs are completed normally and READs execute except for the final output stage. Thus, I_{DD} measurements within a system environment can be made.

Conclusion

DRAM architecture changes enable twice the bandwidth without increasing the demand on the DRAM core and while keeping power low. The evolutionary changes enable DDR2 to operate between 400 MHz and 533 MHz, with the potential of extending to 667 MHz and 800 MHz. A summary of the functionality changes is shown in Table 5.

Table 5: Feature Overview

Feature/Option	DDR	DDR2
Data Transfer Rate	266, 333, 400 MHz	400, 533, 667, 800 MHz
Package	TSOP and FBGA	FBGA only
Operating Voltage	2.5V	1.8V
I/O Voltage	2.5V	1.8V
I/O Type	SSTL_2	SSTL_18
Densities	64Mb–1Gb	256Mb–4Gb
Internal Banks	4	4 and 8
Prefetch (MIN Write Burst)	2	4
CAS Latency (CL)	2, 2.5, 3 clocks	3, 4, 5 clocks
Additive Latency (AL)	no	0, 1, 2, 3, 4 clocks
READ Latency	CL	AL + CL
WRITE Latency	fixed	READ latency - 1 clock
I/O Width	x4/ x8/ x16	x4/ x8/ x16
Output Calibration	none	OCD
Data Strobes	bidirectional strobe (single ended)	bidirectional strobe (single ended or differential) with RDQS
On-Die Termination	none	selectable
Burst Lengths	2, 4, 8	4, 8

Jeff Janzen has been a DRAM applications engineer with Micron's computing and consumer group for five years. Prior to joining Micron, Jeff spent 10 years at Texas Instruments — 8 years in product engineering and 2 years in strategic marketing. Jeff holds a BSEE from Kansas State University.

Modifications to the DRAM architecture include shortened row lengths for reduced activation power, burst lengths of four and eight for improved data bandwidth capability, and the addition of eight banks in 1Gb densities and above. New signaling features include ODT and OCD. ODT provides improved signal quality due to better system termination on the data signals, and OCD calibration provides the option of tightening the variance of the pull-up and pull-down output driver at 18 ohms nominal. Modifications were also made to the mode register and extended mode register, including CAS latency, additive latency, and programmable data strobes.

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Assunto: Re: Pedido de esclarecimento - TST PE 049/2006
De: Serviço de Licitações e Contratos <srlca@tst.gov.br>
Data: Wed, 05 Jul 2006 14:59:43 -0300
Para: Janaina Morbeck Felix <janaina@microlog.com.br>

Prezados Senhores,
Segue em anexo a resposta à consulta formulada.
Atenciosamente,

```
Fabiano de Andrade Lima
Diretor do Serviço de Licitações e Contratos
Tribunal Superior do Trabalho
SAFS – Quadra 8 – Lote 1 – 3º andar - Sala 316 – Brasília – DF
CEP 70.070-600
Tel. – (61) 3314-4049
Fax – (61) 3314-4181
```

fandrade@tst.gov.br

Janaina Morbeck Felix escreveu:

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> Segue anexo pedido de esclarecimento referente ao edital do Pregão Eletrônico nº 049/2006.
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> Att.
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> MICROLOG
>
> Janaina Morbeck Felix
> **Representante Interno de Vendas – Internal Sales Representative**
> Microlog Informática e Tecnologia
> janaina@microlog.com.br
> Phone: +55 (61) 3468-9800
> Fax: +55 (61) 3468-5995

Assunto: Re: [Fwd: Pedido de esclarecimento - TST PE 049/2006]
De: Henrique <jhrfilho@tst.gov.br>
Data: Wed, 05 Jul 2006 15:00:19 -0300
Para: Serviço de Licitações e Contratos <srlca@tst.gov.br>
CC: Mauricio Pena <mpena@tst.gov.br>, Lucio Mafra Martins Teixeira <mafra@tst.gov.br>, Rafael Almeida de Paula <rafaelp@tst.gov.br>, Heron Vieira da Conceicao <heronvc@tst.gov.br>

Sim, está correto o entendimento da empresa Microlog.

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> Conforme regra estabelecida no Decreto nº 5.405/2005, art. 18, § 1º, resposta
> deverá ser formulada por este Pregoeiro em até 24 horas.
> Respeitosamente,
>
> ---
>
> **Assunto:**

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De: "Janaina Morbeck Felix" <janaina@microlog.com.br>
Data: Wed, 5 Jul 2006 14:41:23 -0300
Para: <cpl@tst.gov.br>
Para: <cpl@tst.gov.br>
CC: "Marco Aurelio Silveira de Araujo" <marco@microlog.com.br>

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Segue anexo pedido de esclarecimento referente ao edital do Pregão Eletrônico nº 049/2006.

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```
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José Henrique Rodrigues Filho
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jhrfilho@tst.gov.br
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Brasília-DF, 05 de julho de 2006.

Ao
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Att. Comissão Permanente de Licitação

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MICROLOG INFORMÁTICA E TECNOLOGIA LTDA., empresa estabelecida em Brasília, Distrito Federal, parceira comercial do Fabricante DELL, na condição de postulante à participação no certame em referência, vem, no prazo previsto no Edital do Pregão Eletrônico N° 049/2006, pedir esclarecimentos sobre disposições nele contidas, como seguem:

1. O Edital, em seu Anexo I, Item 2, subitem 13 – Gabinete, letra "b", exige:
   "Fonte de alimentação – entrada de 110 e 220 VAC, chaveada manual e automaticamente ..."

   Entendemos que houve um erro de digitação nesse item e que onde se lê "chaveada manual e automaticamente" lê-se "chaveada manual ou automaticamente". Está correto nosso entendimento?

Sendo o que se apresenta, na oportunidade, e confiando em que haverá acolhida para o esclarecimento que se deseja obter, subscrevemo-nos.

Atenciosamente,

MICROLOG INFORMÁTICA E TECNOLOGIA LTDA.
Marco Aurélio Araújo
Gerente de Contas
marco@microlog.com.br